Additional circuit methods realized under the claims of U.S. Patent 2016/0344401-A1 (Nov. 24, 2016) and related PCT international filings

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Text 4 pages, Drawings 8 pages

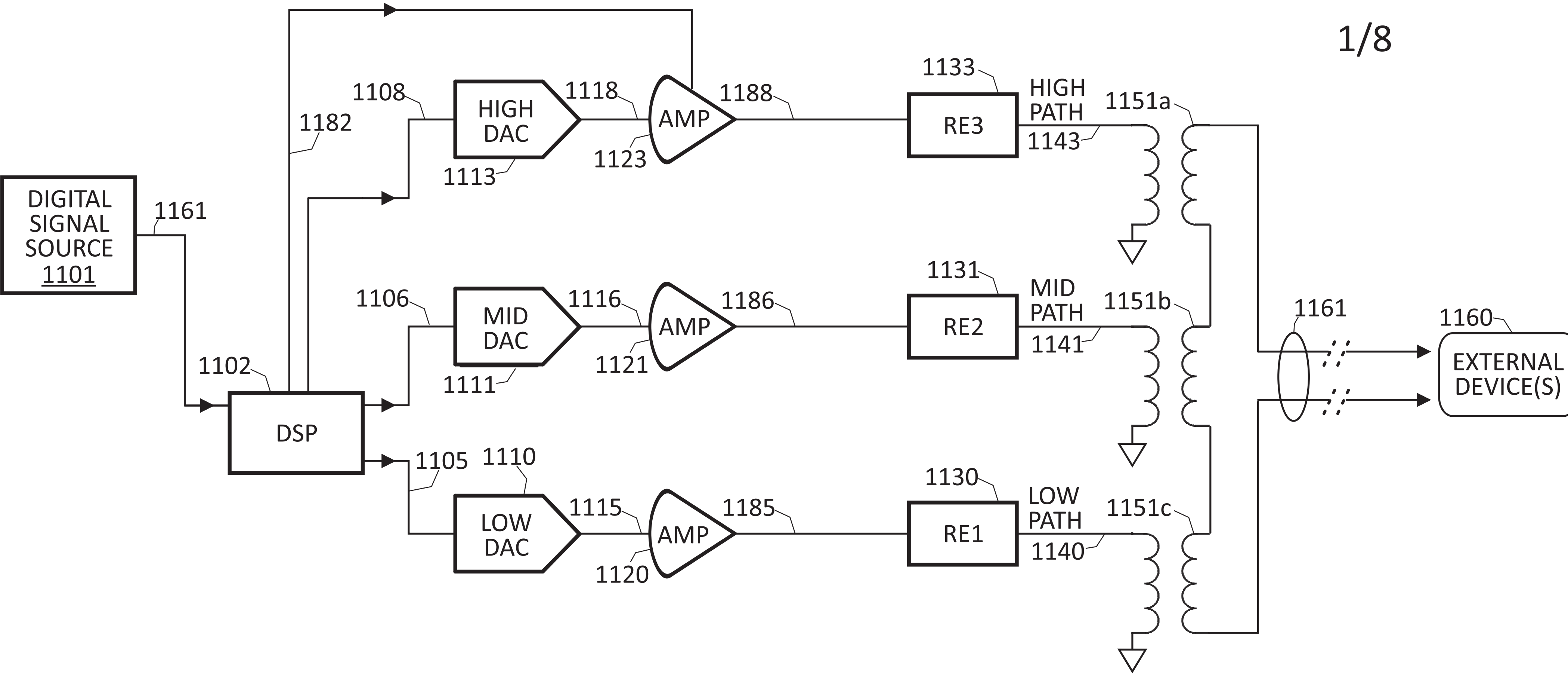
In an embodiment shown in FIG 12J, within the scope of the referenced patent claims, low-path(s) attenuation could be integrated into the transfer function of a transformer (1254) with said low-path transformer (1254) configured for a voltage step-down (level-reduction) and output summing as would be understood by one skilled in the art. In an alternative embodiment shown in FIG. 12J, within the scope of the referenced patent claims, high-path gain, elsewhere achieved by an active element or amplifier (*e.g.,* (1223) of FIG. 12B), is achieved by transformer (1253) configured for a voltage step-up transfer function (level-boost) and output summing as would be understood to one skilled in the art. The single-ended topology shown in FIG. 12J could be achieved with a differential topology. One example of said differential topology is shown in FIG. 12K. In an additional alternative embodiment shown in FIG. 12L, a voltage step-up transformer (1255a) is used for the high-path output signal (1218) and a non-transformer output is used for the low-path output signal (1215)(1240). In an additional alternative embodiment shown in FIG. 12M, a step-down transformer (1257a) is used for the low-path output signal (1215) and a non-transformer output is used for the high-path output signal (1243), along with summing technique(s) as would be understood by one skilled in the art. In an additional alternative embodiment which can be represented by FIG. 11C, low-path gain reduction or attenuation can be shared by any method or combination of methods, including resistive attenuation, step-down transformer, digitally-controlled attenuation, device power-up/power-down state, and so forth, as detailed extensively in the referenced patent, and within the scope of the referenced patent claims. For example, in FIG. 11C, if a total attenuation of -30dB is required on output signal (1185), the resistive element (1130) could exhibit -15dB of attenuation while the transformer (1151c) could also exhibit -15dB of step-down level shift, for a total low-path attenuation of -30dB as seen at (1140). Similarly, in FIG. 11C, if signal (1118) requires an additional total gain of +20dB, the high-path amplifier (1123) could exhibit +10dB of gain while the high-path transformer (1151a) could also exhibit +10dB of step-up level shift, giving a total combined gain of +20dB at the output of transformer (1151a). The claims of referenced patent provide for any combination of common gain boost methods (*e.g.,* active amplifier, step-up transformer, etc.) used in the high-path(s). Likewise, the claims of referenced patent provide for any combination of attenuation or level reduction methods (*e.g.,* attenuator, step-down transformer, etc.) used in the low-path(s).

Transformer input(s) and/or output(s) (i.e., primary/secondary) used within the scope of claims of the referenced patent may be terminated single-ended, differential, grounded, floating, single-in diff-out, diff-out single-in, multi-tapped winding, parallel, series, series-parallel, split, or any other suitable transformer topology as would be understood to those skilled in the art. While alternative level-cut and level-boost techniques are described via the three-path Figure 11C and the two-path Figures 12J, 12K, 12L, and 12M, similar level-cut and level-boost techniques could be used in any number (*n*) of paths (*i.e.,* 2 paths, 3 paths, 4 paths … *n* paths). While the transformers of FIG. 11C are shown configured in a particular combined (summed) secondary technique, the referenced patent and its claims provide for any transformer or hybrid combining (summing) technique (*i.e.,* transformer + non-transformer, etc.) that achieves summation of multiple paths while maintaining low noise and high dynamic range. Similarly, while multiple transformers are shown with a single transformer dedicated to each path (*e.g.,* FIG. 12K, etc.), a single physical transformer structure with multiple windings and/or cores and/or taps and/or primaries and/or secondaries could be used with multiple paths, the design of such would be understood by one skilled in the art. While resistive elements may be shown in low and high paths (*e.g.,* FIG 11C: RE1, RE2, RE3), resistive elements in each path (if required) may be achieved in whole or in part by the DC resistance and/or AC impedance of the transformer(s). While high-path(s) noise switching techniques may be used between DAC output and transformer input, the referenced patent claims provide for high-path(s) noise reduction or removal anywhere in said path(s), including directly before a transformer winding, directly within a transformer winding or transformer body structure, or directly after a transformer winding, or some combination thereof.

As noted in the reference patent, DAC devices often employ differential outputs. An example of differential low-path and high-path is shown in FIG. 12N, showing DACs (1210a) and (1213a) with differential outputs (1215a) and (1218a) feeding the inputs of differential amplifiers (1224) and (1223), respectively. Also in FIG. 12N, output-summing transformers are shown with dual windings on both primary and secondary, which are shown tied in a common series configuration. FIG. 12P shows alternative high-path(s) noise control methods (under digital control, as described in the referenced patent) which shunts the high-path transformer primary winding(s) via switching element (1285), or shunts the high-path transformer secondary winding(s) via switching element (1286), or shunts both the primary and secondary winding(s) of the high-path(s) transformer(s), as described by the claims of the referenced patent with respect to the function and control or high path(s) noise-removing or noise-reducing elements. If more than one higher path requires noise management, then such noise management switching can be applied to each required path in the appropriate manner as described by claims of the referenced patent. While noise reduction or removal by the shunting of transformer primary and/or secondary winding is shown in FIG. 12P in conjunction with a differential signal path, shunting of transformer winding can also be achieved in a single-ended signal path. When the high-path transformer primary and/or secondary winding is shunted by any of these methods, the noise of the upstream feed device(s) (*e.g.,* DAC, Amplifier, etc.) can also be reduced or removed from the circuit for potentially improved noise reduction at the summing output, as described in the referenced patent.

FIG. 12Q shows a simplified example of differential high and low signal paths using transformer summing in a manner that employs multiple primary windings in a feedback topology. Myriad types of transformer-amplifier feedback topologies are well-known to those skilled in the art and may provide improved electrical performance (examples include US4614914, DE2901567, DE3304136, US4453131A, Jensen Transformers application schematics AS025 and AS051, etc.). One example of transformer feedback is shown in FIG. 12Q and will indicate that the broadest range of primary feedback techniques can be used under the scope of the claims of the referenced patent. In the example shown in FIG. 12Q, common feedback elements have been omitted for simplification, such as required feedback and feed-forward resistances, compensation capacitance, additional primary windings with additional feedback/feed-forward paths, and so forth – the details of which would be understood to those skilled in the art. While an example of amplifier-transformer feedback topology is shown in a differential signal path, transformer feed-back functionality can be achieved using single-ended signal paths, or differential-single hybrids, as shown by the prior-art examples above and elsewhere.

As shown in FIG. 12R, and in reference to methods described in the referenced patent, and under the claims of the referenced patent, in a differential signal path, a shunting element (1290) (digitally-controlled or otherwise) can also be used upstream of the high-path(s) resistive element(s) for high-path(s) noise-reduction or noise-removal (*i.e.,* in a single-ended signal path, the shunt element can be routed to ground or common, not shown here). Under the claims of the referenced patent, any variation of series path switching and/or shunt techniques can be used to reduce or remove path noise from the summing output, including but not limited to shunting of primary and/or secondary windings in transformer output, differential shunt, single-ended shunt to common or ground, both differential paths shunted to ground (*i.e.,* positive and negative paths in a differential signal both shunted to ground or tied common or some variation thereof), shunt or series switching techniques in consort with other noise reduction or removal techniques (*e.g.,* digitally-controlled power cycling of active devices, digitally controlled resistive or attenuation devices, etc.), and myriad combinations of above switching and/or shunting known to those skilled in the art.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1102
DSP
1182
1108
HIGH DAC
1113
1118
AMP
1123
1188
1106
MID DAC
1111
1116
AMP
1121
1186
1105
1110
LOW DAC
1115
AMP
1120
1185
1133
RE3
HIGH PATH
1143
1131
RE2
MID PATH
1141
1130
RE1
LOW PATH
1140
1151a
1151b
1151c
1161
1160
EXTERNAL DEVICE(S)

FIGURE 11C

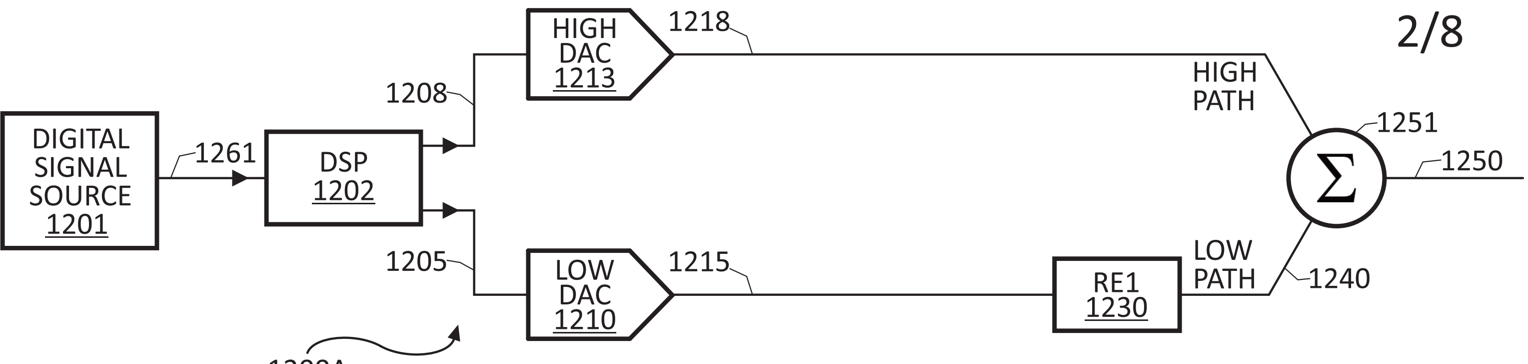

FIGURE 12A

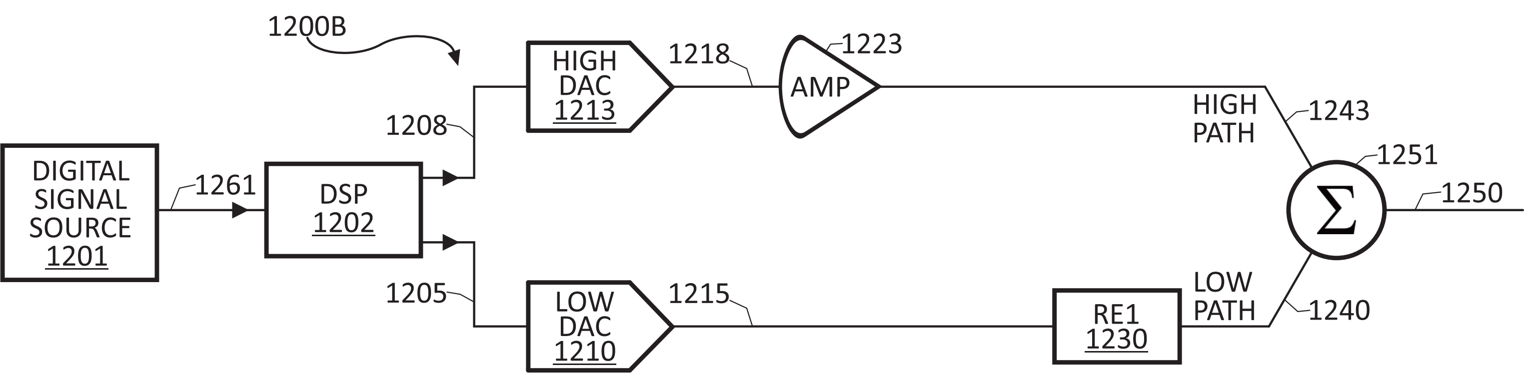

FIGURE 12B

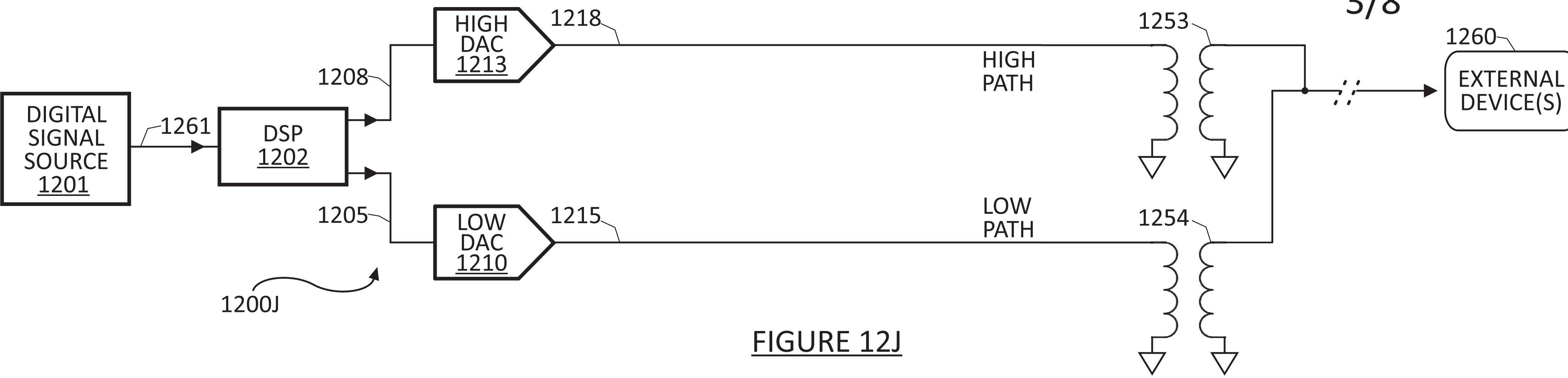

FIGURE 12J

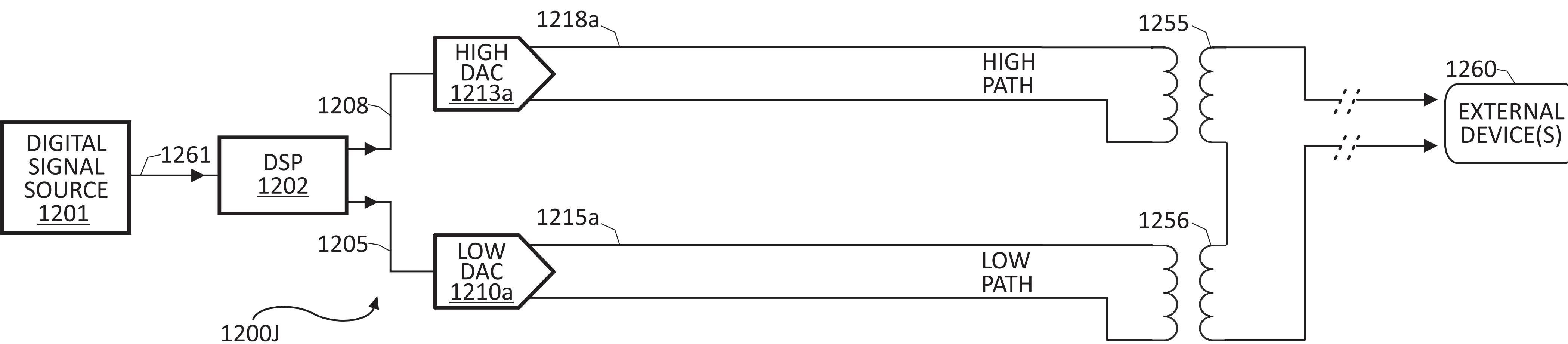

FIGURE 12K

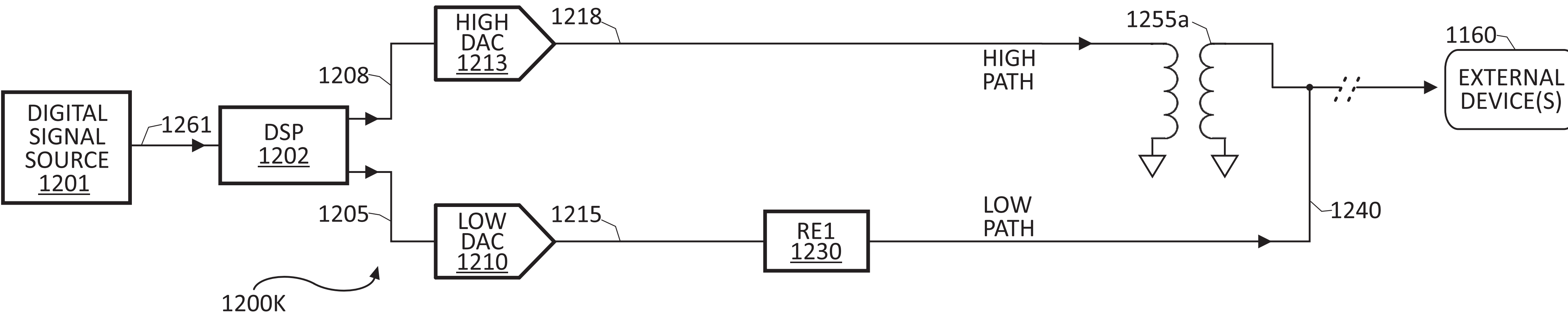

FIGURE 12L

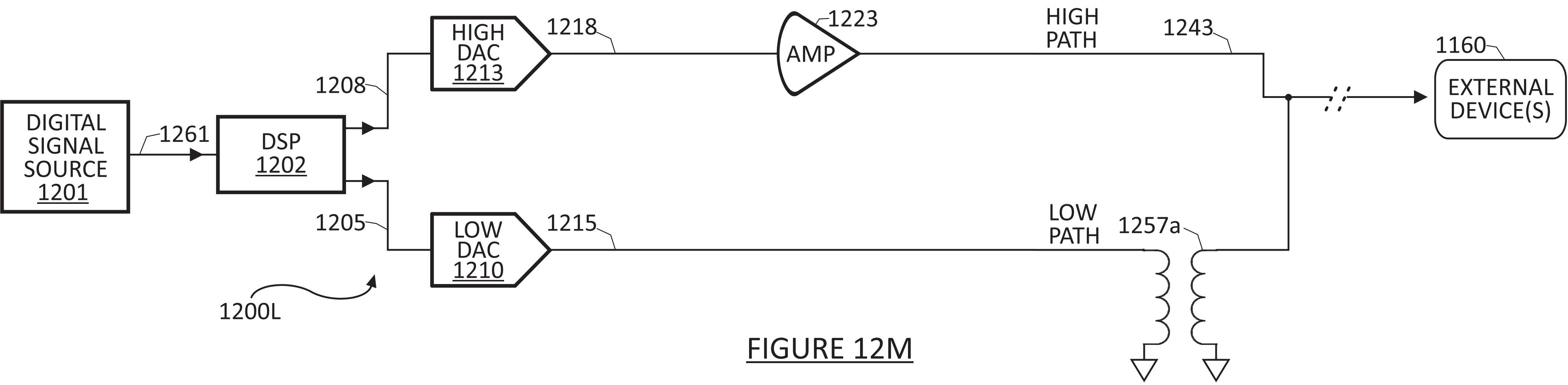

FIGURE 12M

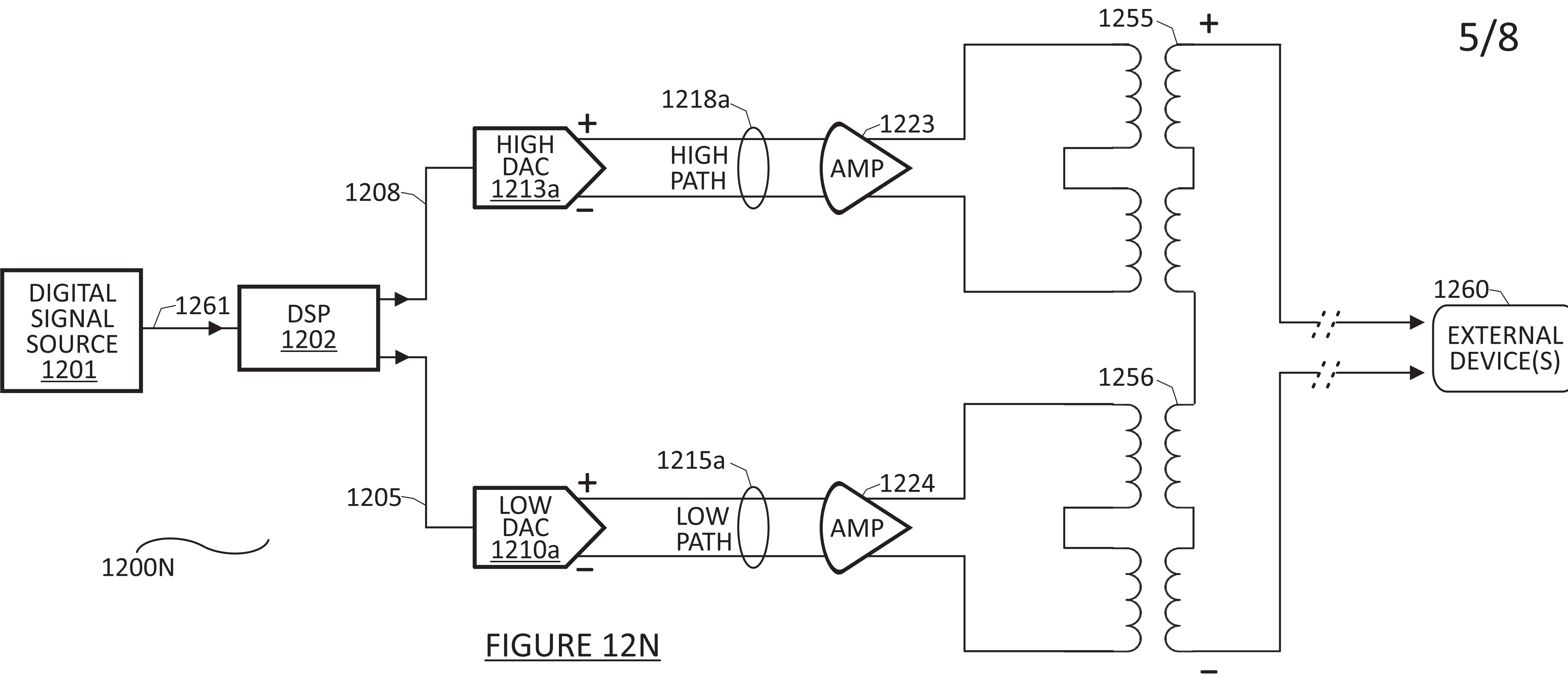
DIGITAL SIGNAL SOURCE 1201
1261
DSP 1202
1208
1205
HIGH DAC 1213a
LOW DAC 1210a
+
−
1218a
HIGH PATH
1215a
LOW PATH
AMP
1223
1224
1255
1256
+
−
1260
EXTERNAL DEVICE(S)
1200N

FIGURE 12N

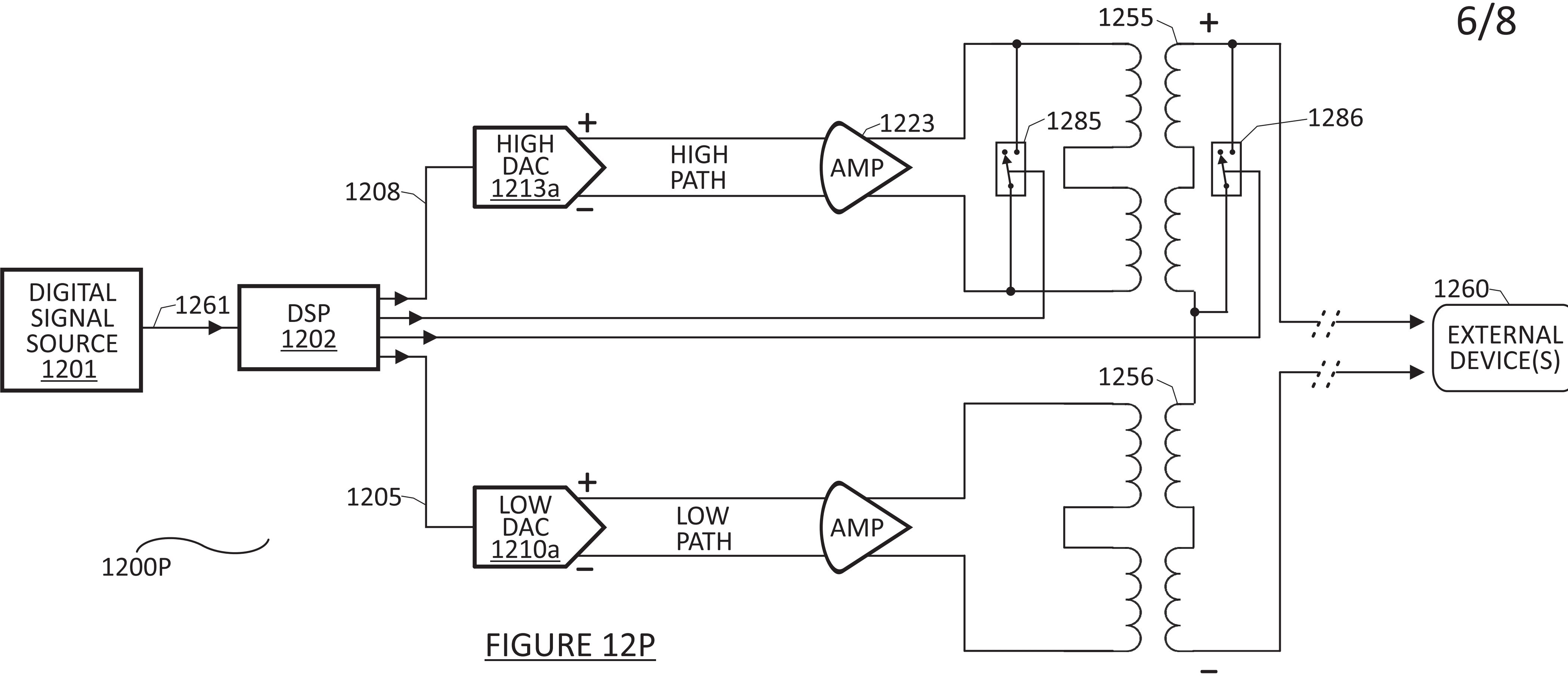
DIGITAL SIGNAL SOURCE 1201
1261
DSP 1202
1208
HIGH DAC 1213a
HIGH PATH
AMP
1223
1285
1255
1286
1260
EXTERNAL DEVICE(S)
1256
1205
LOW DAC 1210a
LOW PATH
AMP
1200P

FIGURE 12P

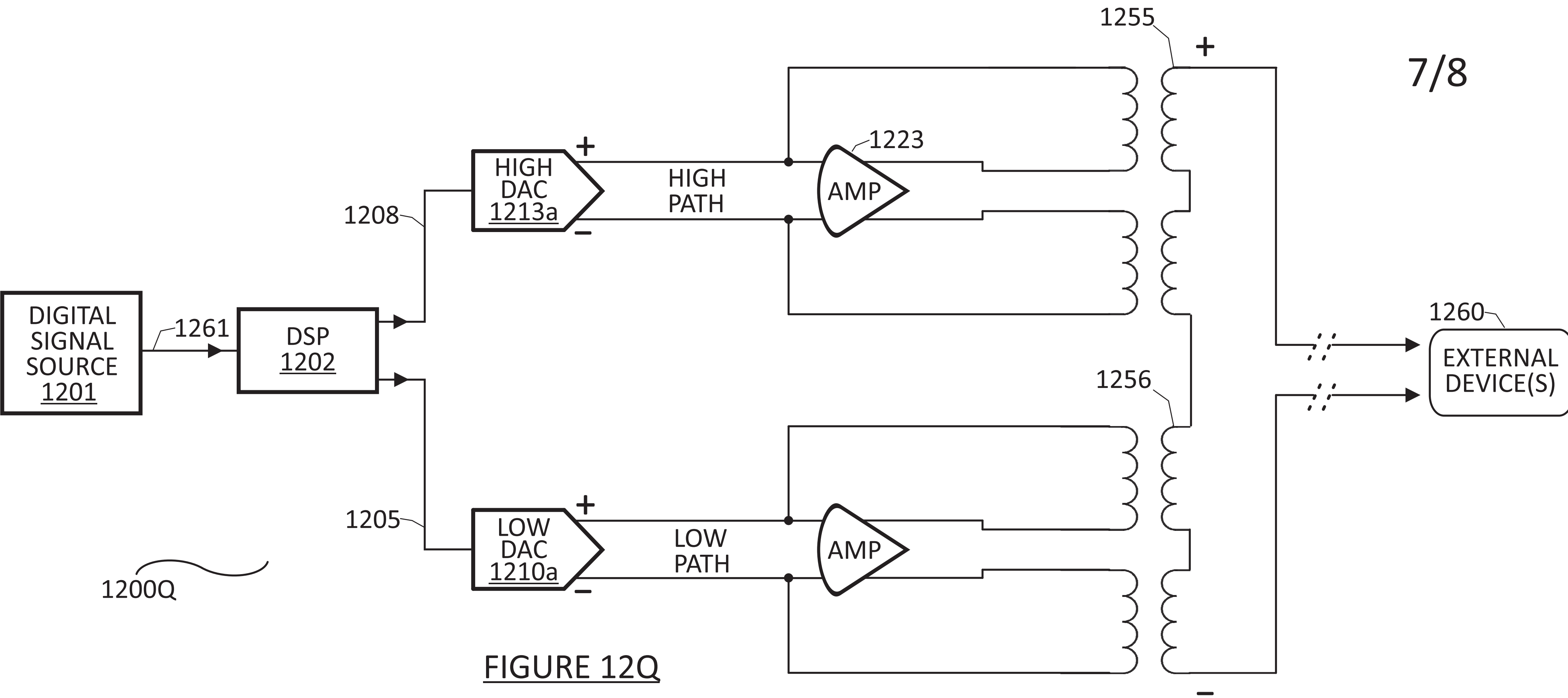
DIGITAL
SIGNAL
SOURCE
1201
1261
DSP
1202
1208
1205
HIGH
DAC
1213a
LOW
DAC
1210a
+
−
HIGH
PATH
LOW
PATH
AMP
1223
AMP
1255
1256
+
−
1260
EXTERNAL
DEVICE(S)
1200Q

FIGURE 12Q

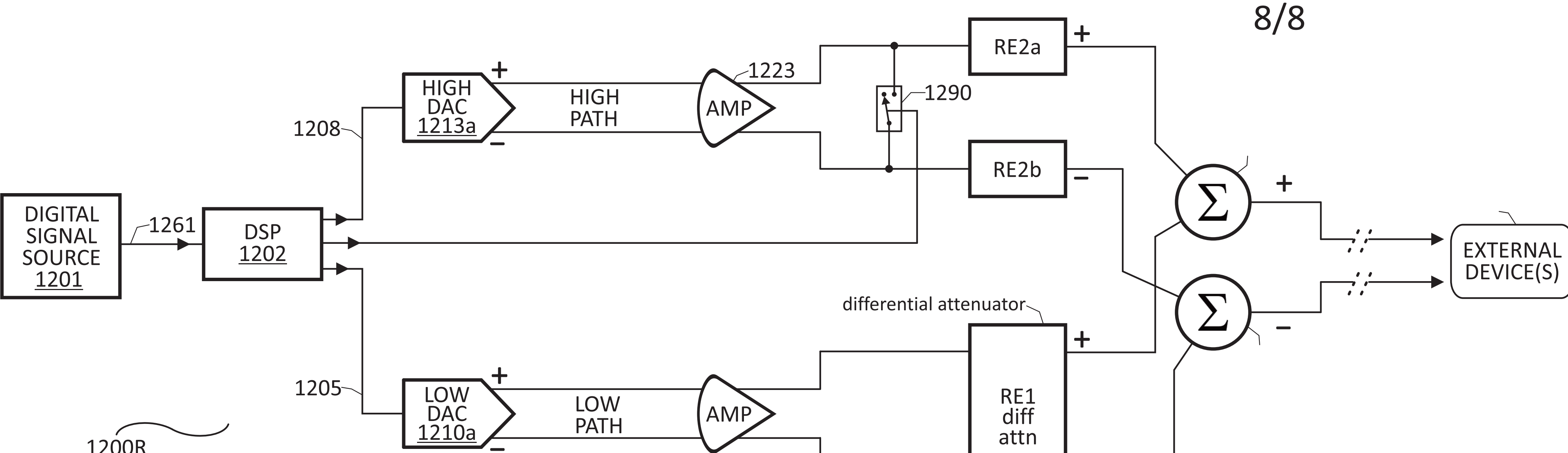
DIGITAL
SIGNAL
SOURCE
1201
1261
DSP
1202
1208
HIGH
DAC
1213a
+
−
HIGH
PATH
AMP
1223
1290
RE2a
RE2b
+
−
Σ
Σ
+
−
EXTERNAL
DEVICE(S)
1205
LOW
DAC
1210a
LOW
PATH
AMP
differential attenuator
RE1
diff
attn
1200R

FIGURE 12R